Sequential Circuit Design in Quantum Dot Cellular Automata

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Abstract

In this work we present a novel probabilistic modeling scheme for sequential circuit design in Quantum-Dot Cellular Automata(QCA) technology. Clocked QCA circuits possess an inherent direction for flow of information which can be effectively modeled using Bayesian networks (BN). In sequential circuit design this presents a problem due to the presence of feedback cycles since BN are direct acyclic graphs (DAG). The model presented in this work can be constructed from a logic design layout in QCA and is shown to be a dynamic Bayesian Network (DBN). DBN are very powerful in modeling higher order spatial and temporal correlations that are present in most of the sequential circuits. The attractive feature of this graphical probabilistic model is that that it not only makes the dependency relationships amongst node explicit, but it also serves as a computational mechanism for probabilistic inference. We analyze our work by modeling clocked QCA circuits for SR F/F, JK F/F and RAM designs.

I. Introduction

Quantum-Dot Cellular Automata(QCA) is one of the most promising nanotechnology that uses a novel computational paradigm to perform computations by device to device interaction rather than transfer of charge. A simple QCA cell can be represented as a quantum well with four dots. Two electrons in the quantum well occupy the diagonal dots to represent a two state system. Information is transferred between individual QCA cells by device to device columbic interactions. In any QCA circuit the required operation can be readily observed by understanding the functionality of a Quantum-dot and the majority gate; however the thermal and polarization effects are not seen clearly as well as its functionality. This requires a model that could be used to observe these effects more reliably.

Among different types of QCA designs, modeling sequential circuits, which happens to be the most common type of logic is the hardest. This is particularly due to the higher order spatial and temporal dependencies mainly caused by the presence of feedback components. In order to model this we make use of an important first order Markov property, i.e. the system state is independent of all past states given just the previous state.

The inputs to a sequential circuit are not only the primary inputs but also these feedback signals. The feedback lines can be looked upon as determining the state of the circuits at each time instant. Given a set of inputs i_t and present states s_t, the next state signal s_{t+1} is uniquely determined as a function of i_t and s_t. At the next time instance, we have a new set of inputs i_{t+1} along with state s_{t+1} as an input to the circuit to obtain the next state signal s_{t+2}, and so on. Hence, the statistics of both spatial and temporal correlations at the state lines are of great interest. It is important to be able to model both kinds of dependencies in these lines.

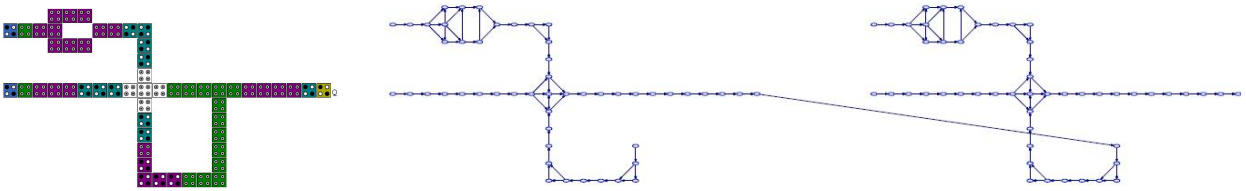
While it has been shown how combinational QCA logic circuits are probabilistically modeled using normal BN [1], sequential circuit design presents a problem due to the presence of feedback loops. A BN is a DAG probabilistic model that could effectively represent circuit probabilities at ground state and near ground state configurations. The representation of a BN of the same circuit at various time slices without the feedback path is known as a dynamic BN which is detailed in Section IV. We analyze the effect on polarization in sequential circuits due to various circuit dependencies using DBN. We design the circuit using QCA designer [2] and realize the layout in GeNIe [3] as a DBN.

II. Prior Work

Most of the works in QCA use combinational logic to build ALU, microprocessors and FPGA where the effect of polarization is not a major factor but memory circuits like RAM [2], [4], [5] have greater effect on polarization due to the sequential nature and requires analysis to determine optimal conditions that will aid the efficiency of such systems. Similar study has been performed experimentally on sequential circuits to observe the decay and switching errors [6]. Earlier works in sequential circuits tested the designs for fault conditions due to missing or additional cells and timing constraints associated with QCA clocking and have proposed an algorithm to match the clocking zones such that the output arrives at the same time, known as the stretching algorithm [7]. In this work, we extend the study of functionality, polarization, thermal dependencies and cell-size dependencies for sequential circuits.

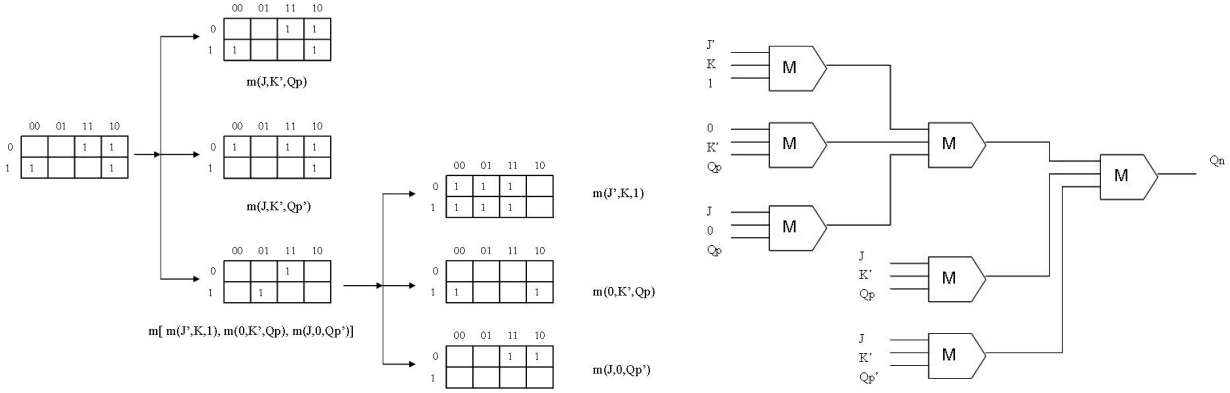
III. Sequential QCA Circuits

Fig. 1(a) shows the SR F/F proposed in [8] which is also used for the validation of our model. We designed the circuit for JK F/F using majority gate reduction from its Karnaugh map. Fig. 2 shows the K-map reduction, corresponding



(a) (b)

Fig. 1. (a) SR F/F design proposed by [8] (b) Dynamic Bayesian model



(a) (b)

Fig. 2. (a) Majority gate reduction for JK F/F (b) Resulting majority gate model

schematics and Fig. 3 shows the QCA layout. It consists of 7 majority gates and looks similar to a QCA adder circuit.

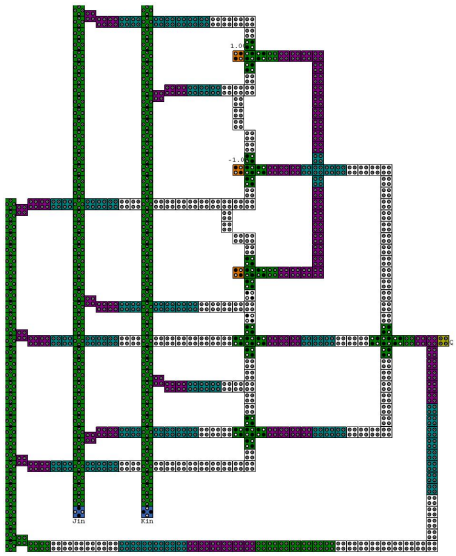


Fig. 3. QCA JK F/F layout

We make use of the RAM (Fig. 4) proposed in [2] to analyze the polarization effects in the feedback path. The 'write' operation in an ideal RAM will have the input value circle the feedback loop while the output remains unaffected. So if the input value is 0/1 then the value is fed back until there is a change in the input or during a read interrupt signal else the output remains 0. During the 'read' operation the output follows the current value in the feedback irrespective of any change in the input.

IV. Dynamic BN Approach

DBN is useful to study the effect of sequential circuits represented as a dynamic time coupled BN. Much like the special case formalisms such as hidden Markov models and linear dynamic systems, DBN handles dependencies between various time slices without disturbing the internal dependencies using random set of variables. If t_i represent the time slice at i_{th} instance and the underlying dependencies for the combinational part is represented as a function of nodes V_{t_i} and links E_{t_i} at time slice t_i as $G_{t_i} = (V_{t_i}, E_{t_i})$, then the nodes of the DBN could be represented as a union of all nodes for each time slice.

$$V = \bigcup_{i=1}^{n} V_{t_i} \tag{1}$$

However the links of a DBN E includes both the union of the links for one time slice and the temporal edges (links connecting two time slices) $E_{t_i,t_{i+1}}$, defined as

$$E_{t_i,t_{i+1}} = \{(X_{i,t_i}, X_{j,t_{i+1}}) | X_{i,t_i} \in V_{t_i}, X_{j,t_{i+1}} \in V_{t_{i+1}}\} \tag{2}$$

Where X_{j,t_i} is the j-th node of the DAG for time slice t_i. Even in a generalized structure, where the temporal edges can be between any node from the time slice t_i to any node of time slice t_{i+1}, the overall structure must represent the minimal Identity map of the underlying model (Fig. 1(b).

Any feedback circuit could be looked as an infinite series of identical combinational circuits getting their input values from the previous circuit. The method of opening the feedback

loop into identical circuits operating at different time slices is known as $unraveling$. Based on the underlying Markov property, we give arbitrary values to the circuit at the first time slice and connect the rest in series by coupling the output of the circuit in the previous time slice as the feedback input of the circuit at the next time slice (Fig. 1(c)).

The complete set of edges E is

$$E = E_{t_1} \cup \bigcup_{i=2}^{n} (E(t_i) + E_{t_{i-1},t_i}) \tag{3}$$

The conditional probabilities that we need for DBN models use the density matrix formulation to arrive at the steady state probability as derived in [1] is given by;

$$\begin{aligned} P(X = 0|pa(X)) &= \rho_{11}^{ss}(pa(X), ch^*(X)) \\ P(X = 1|pa(X)) &= \rho_{22}^{ss}(pa(X), ch^*(X)) \end{aligned} \tag{4}$$

The polarization of the electrons in the cell can be obtained from the difference between the two conditional probabilities as;

$$Polarization\ P = P(X = 0|pa(X)) - P(X = 1|pa(X)) \tag{5}$$

We compare the polarization calculated using Eq. 5 with the polarization value obtained from the QCADesigner (as shown in Table I). In view of the fact that the model presented calculates the worst case polarizations, the polarization obtained from this method is a little pessimistic than that obtained from the QCADesigner simulation as.

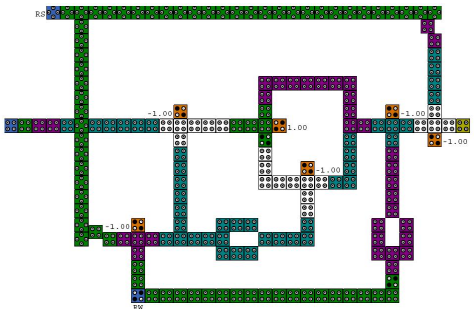


Fig. 4. RAM proposed in [2]

V. Results and Discussion

We obtained the results from the DBN model generated in GeNIe [3] for effects on polarization due to temperature and circuit geometry. First we discuss the validation of our model and then discuss the results obtained through the analyses. Sequential circuits depend on the current input values and the previous output value so if the input does not switch, the value in the feedback or at the output remains the same. As we study the effect of polarization having same inputs may not help much in observing the effect. Effect on polarization is better observed when the input switches from one state to the other. We therefore vary the inputs to see the stability of the output at each time slice in terms of polarization of the cell. We set the inputs to '1' for logic $High$ and '-1' for logic Low.

S	R	Q_n
0	0	-1
1	0	1
0	0	1
0	1	-1
0	0	-1

(a)

Q_p	S	R	Q_n
-1	-1	-1	-1
-1	1	-1	0.988
0.998	-1	-1	0.987
-1	-1	1	-0.994
-0.994	-1	-1	-0.992
1	-1	-1	0.989
0.989	-1	-1	0.977

(b)

TABLE I

(a)Results from QCADesigner (b)Results from BN model

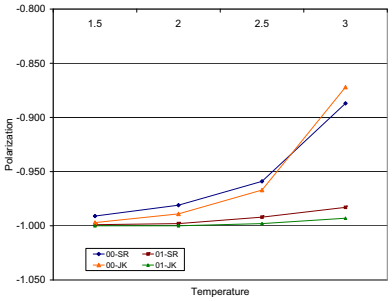


Fig. 5. Drop in output Polarization in F/F when the input is low

A. Ground Truth

We validate our model by simulating the circuit (Fig. 1(b)) in QCADesigner for the ground truth. We use coherence vector approximation engine and a vector table type simulation with inputs shown in Table I(a) and the output polarization was observed in Q_n. We compared the results obtained through DBN model (Table I(b)) and observe that the results are almost similar. The simulation time was 65 seconds in QCADesigner while the BN model took only 0.3 seconds in a Intel Core^{TM} Duo 2.13 GHz CPU with a RAM size of 4GB.

B. Effect of Working Temperature

We vary the temperature in steps to observe its effect on the polarization of the cell. Fig. 5 shows the graph plotted for the drop in polarization at the output of the F/F while it goes low. We observe that during the reset operation both the F/F show very less decay in polarization even at high temperatures, but when both the inputs are low the decay in polarization increases as the temperature increases. When the output is high (Fig. 6) we observe that in the SR F/F during a high Set input, the output decays linearly with temperature but on the other hand the JK F/F decays much faster. During the condition when both JK inputs are high, the output drops exponentially and as for SR the condition is an invalid condition.

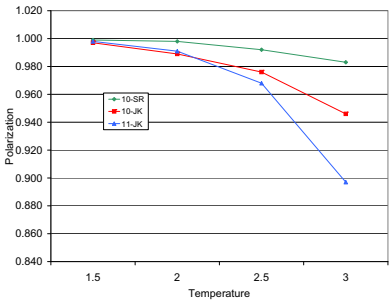


Fig. 6. Drop in output Polarization in F/F when the input is high

S	R	Q_n	
		18nm	9nm
-1	-1	-1	-1
-1	1	-0.994	-1
1	-1	0.988	1
1	1	-0.977	-1

(a)

J	K	Q_n	
		18nm	9nm
-1	-1	-0.96	-1
-1	1	-0.998	-1
1	-1	0.976	1
1	1	0.960	1

(b)

Q_P	I/P	$RAMCellSize = 18nm$		$RAMCellSize = 9nm$	
		Read	Write	Read	Write
-1	-1	-0.995	0.891	-1	-1
-1	1	-0.983	0.992	0.999	-1
1	-1	0.879	-0.985	-1	1
1	1	0.891	0.868	0.999	1

(c)

TABLE II

(A) COMPARISION OF SR F/F [8] (B) COMPARISON OF JK F/F (C) COMPARISON OF RAM

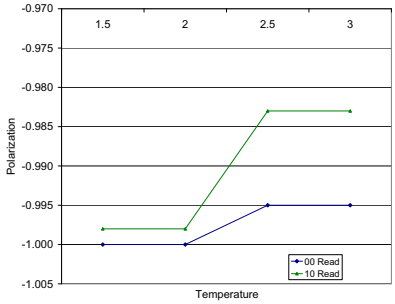


Fig. 7. Drop in output Polarization in RAM during read operation when the feedback input is low

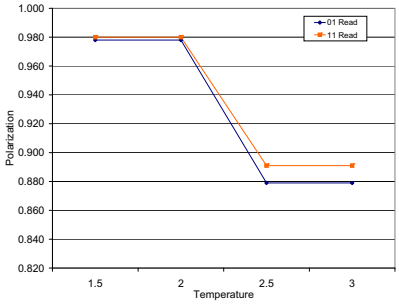


Fig. 8. Drop in output Polarization in RAM during read operation when the feedback input is high

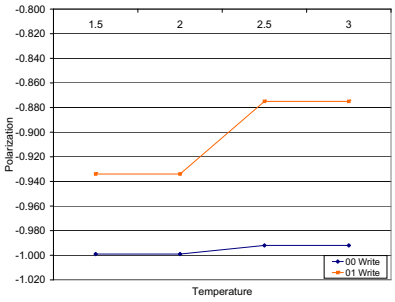


Fig. 9. Drop in output Polarization in RAM during write operation when the feedback input is low

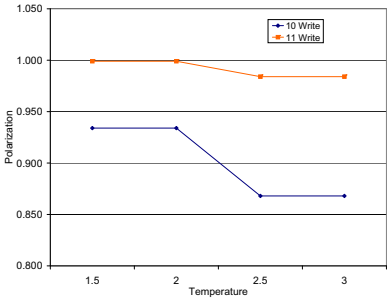


Fig. 10. Drop in output Polarization in RAM during write operation when the feedback input is high

Fig. 7- 10 shows the results from the RAM circuit during read and write operation, we observe that the data in the feedback loop does not lose its polarization unless the input switches.

C. *Effect of Circuit Geometry*

We performed analyses on circuits designed using Type 1 cell with dimensions of 18nm and dot diameter of 5nm and Type 2 cell with dimensions half of the former and the dot diameter of 2nm. The environment variables set for the analysis were; clock high $1.0e^{-21}$ clock low $3.0e^{-34}$ grid spacing $10nm$ for Type 1 cells and $5nm$ for the Type 2 cells. Table II(a) shows the results obtained from circuit with the $18nm$ cell size for SR F/F we observe that scaling down the dimensions by half produces more stable results. From Table II(b) we observe that even with the large number of cells JK F/F shows pretty stable results. Table II(c) shows the results obtained with the RAM in read and write mode.

VI. CONCLUSION

We analyzed sequential logic circuits in QCA using a novel probabilistic modeling scheme. We used a graph unraveling technique to determine the output of sequential circuits based on the working temperature and the device geometry factors that affect its polarization. The circuit could be replicated any number of times to study the cumulative of 'N' number circuits at different time slices. We have also shown that our model is fast by validating it with QCADesigner using a basic SR F/F.

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