Work in Progress: Introduction of K-map based Nano-logic Synthesis as Knowledge Module in Logic Design Course

Saket Srivastava and Sanjukta Bhanja
Electrical Engineering, University of South Florida,
Tampa, FL - 33613 (ssrivast, bhanja)@eng.usf.edu

Abstract – **This work in progress reports an effort of introducing knowledge module regarding novel nano-devices and novel logic primitives in undergraduate logic design class. Our motivation is to make our students aware of fundamental abstracted logical behaviors of future nano-devices, their functionality. This effort would also help the students use their existing knowledge of K-map based logical synthesis into constructing logic blocks for novel devices that uses majority logic as basic construct. Moreover, additional to stimulating our students' interests, we are also augmenting their learning by challenging them to use their existing knowledge to analyze, synthesize and comprehend novel nano-logic issues through the worksheets and lecture modules. Whereas many efforts are focusing on developing new courses on nanofabrication and even nano-computing, we intend to augment the existing standard EE and CS courses by inserting knowledge modules on nano-logic structure for stimulating their interest without significant diversion from the course framework.**

Index Terms – Nano-logic, K-map, Logic Design.

INTRODUCTION

As it is predicted that technology scaling of CMOS would stop somewhere around the year 2020, it is highly likely that current students in computer engineering (CE) would have to design and grapple with nano-level devices and design related issues in a relatively near time frame. Even though CE curriculum and course development needs to address this renewed focus in the longer term, we intend to develop a shorter term strategy, i.e. to augment existing courses with nano-computing related materials. This WIP effort concentrates on Logic Design course in particular introducing the concept of majority/minority logic and using K-map to graphically synthesize small circuits augmenting the standard AND-OR logic by K-map. Note that majority/minority logic is logic primitive for Quantum-dot-cellular-automata (QCA) [2], Single-Electron-Transistor (SET)[3].

We introduced the concept of majority network following the K-map based logic minimization techniques for AND-OR logic. Since our intention is to insert the knowledge module with least diversion, this was the right context to have the seamless introduction to nano-computing. The educational experiments are set to not only expose the students to newer technology but also to test the synthesis and comprehension skills on the learnt K-map in the previous lectures. The knowledge module consists of three parts. First part deals with acquisition of new information regarding nano-devices and learns the logic primitives for such technologies. Second part helps them analyze the information and use them in familiar K-map logical concepts and perform simple analysis. Third part of this knowledge module uses the knowledge obtained in the first two parts to perform a higher level synthesis and comprehension. At each step our aim is to provide a smooth transition within each stage of the module to maximize the learning by applying the logic design concepts that they are familiar with.

At each step we evaluated the learning progress by providing worksheets to the students. We found the results of the worksheets and the feedback survey to be extremely encouraging both to us and to the students. We discuss the results in detail in the Evaluation section.

K-MAP BASED KNOWLEDGE MODULE

K-maps are one of the most essential elements of any Digital logic design curriculum. They facilitate learning by representing information in a graphical format that is easier to comprehend, analyze and to evaluate. The methodology used by us helps our students empower the concepts they have learned about K-maps and then apply them to novel logic styles. Not only do we want the students to learn about new technologies and the logic associated with them, we also want this learning curve to be as smooth as possible, to facilitate better understanding and mostly importantly, to generate greater interest amongst students. We introduce this knowledge module right after the students have acquired significant knowledge on logic expression and logic minimization using K-maps.

Our teaching methodology is threefold. First, students are demonstrated how they can relate the logic associated with other nano-devices in terms of Boolean logic they learn in the Logic design class. This step helps the students grasp the underlying idea behind the new information and relate it to the information they have learnt in the previous lectures of this class.

Secondly, students are shown how they can use this acquired knowledge to analyze the new logic style by making use of a simple AND/OR mapping scheme. Since students are already familiar with AND/OR gates, they find it really interesting how the same type of analysis can be performed using majority logic. This step helps the students visualize and analyze the new logic style with a minimum diversion and to the maximum effect as we will se when we discuss the results of the worksheets handed out to the students for each step in this module. While NAND/NOR logic is considered universal logic style in

CMOS, similarly using a majority gate and inverter one can synthesize any logic circuit in QCA. It is important for students to realize this concept that while logic styles might change when technology changes, but the inherent concepts regarding design styles remain the same.

As a final part of this logic module, we ask the students to perform a relatively complex synthesis algorithm by applying the K-map knowledge they have acquired from the previous lectures in this course to the new logic style that they have learnt from this module. The synthesis algorithm [1] was first demonstrated to the students with some examples and then students were asked to synthesize a different circuit based on that. This final step provides a crucial hint to the level of understanding and scope of this knowledge module. In the next section we will evaluate the impact of this knowledge module based on the performance of students in each of the worksheets handed out to them.

EVALUATION

In order to evaluate the level of understanding that students gained from this course module, they were given worksheets at the end of each step of this knowledge module. **Worksheet-1** evaluated their understanding of QCA majority logic. This worksheet gives us idea about the interest and the level of understanding shown by the class to the new concepts. For the students, this worksheet evaluates knowledge retention of the newly acquired ideas and applying it in a novel fashion.

Worksheet-2 evaluates their level of understanding to perform AND/OR mapping of simple Boolean expressions. This worksheet helps the students to not only perform simple synthesis, but also evaluates the seamless transition between known concepts using old logic style to a novel logic style. It helps them visualize how the same circuits that they have been implementing using AND/OR logic be implemented using majority logic by just setting the value of one of the input to zero or one.

Finally, in **worksheet-3,** students were asked to perform a K-map based synthesis method to reduce a complex three input logic function. Students were also asked to perform an AND/OR mapping for the same function to understand the advantage of K-map based method over AND/OR mapping method. This worksheet challenges the analytical skills of the students to apply the knowledge attained in this course to a totally new logic style and also enhances their critical thinking by reinforcement of known ideas. They see how K-maps while being an important part of logic design curriculum can also be used as a synthesis tool for other logic styles.

In **worksheet-1**, 81.25% students were able to complete each problem. In **worksheet-2**, 68.75% students were able to complete each problem while 31.25% students did a part of problem wrong. **In worksheet-3**, 37.5% students were able to complete each problem, 25% students were able to complete K-map based synthesis but were not able to do the AND/OR mapping for the same.

TABLE I
RESULTS OBTAINED FOR EACH WORKSHEET

Worksheet	Percentage of students receiving grade		
	A	B	C
1	81.25	18.75	0
2	68.75	31.25	0
3	37.5	25	37.5

This was the first semester (Fall 2006) that we conducted this study. At the end of the semester we conducted a survey of the student's response. The most important feedback that we obtained was Question-2, where an overwhelming 87% of the students were able to use K-map knowledge for majority logic synthesis. Around 30% could do it easily while more than half the class could do it with some effort. The other feedbacks that we received show that students are very keen to learn more about nanotechnology and logic associated with it.

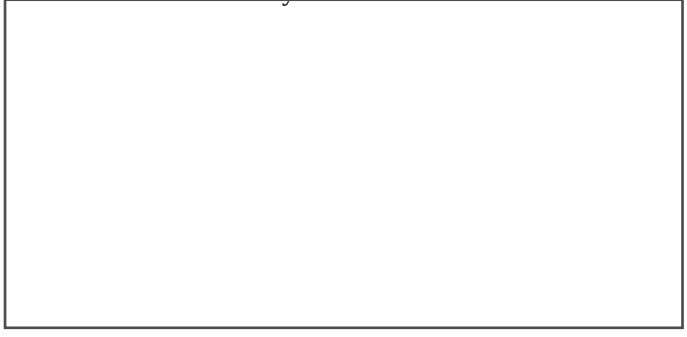

FIGURE 1
SURVEY QUESTIONS: Q1 - HOW DID YOU FIND THE LECTURE ON NANO LOGIC? Q2 - HOW COMFORTABLE YOU WERE IN EXTENDING K-MAP KNOWLEDGE AND APPLY IT TO NANOTECHNOLOGY? Q3 - HOW WELL DID YOU COMPREHEND THE LECTURES? Q4 - HOW DID YOU FIND WORKSHEET ASSIGNMENTS ON LOGIC FLOW IN QCA? Q5 - WOULD YOU HAVE LIKED TO HAVE MORE CLASSES ON NANO-LOGIC DEVICES? Q6 - DO YOU THINK THESE LECTURES WERE HELPFUL IN MOTIVATING YOU TO STUDY MORE ON THESE DEVICES? Q7 - DO YOU THINK NANO-LOGIC SHOULD BE MADE A PART OF CURRICULUM IN FUTURE LOGIC DESIGN CLASSES?
ANSWERS: (A) EXCELLENT (B) GOOD (C) FAIR (D) BAD/DON'T CARE

CONCLUSION

We believe that this module will serve as a good resource for faculties teaching logic design class. The deliverables of this work are the lecture notes, sample student worksheets and feedbacks. The sample worksheets and tutorials presented in class are posted on the web at www.eng.usf.edu/~ssrivast/teaching.htm. In future semesters we also intend to introduce students to other promising nano-logic devices such as SET and Tunneling Phase Logic (TPL) and logic associated with them.

We would like to thank students of undergraduate logic design class to help us perform this study and provide us with the feedback. The student datasets, knowledge module and other resources would be available through computing server resources funded by NSF CNS-0551621, also partially funded by NSF CAREER award CCF-0639624

REFERENCES

[1] Zhang R; Gupta, P; Jha, N K, "Synthesis of majority and minority networks and its applications to QCA, TPL and SET based nanotechnologies," *18th International Conference on VLSI Design*., 3-7 Jan. 2005, pp. 229- 234

1] QCADesigner,"www.qcadesigner.ca"